IN THE ABSTRACT

Please amend the abstract to read as follows:

- - In an SOI MOSFET device, with a silicon layer formed on a dielectric layer, a gate electrode stack is formed, with sidewall spacers ~~located~~ on sidewalls thereof, on the surface of the silicon layer. Raised source/drain regions are formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode ~~formed~~ composed of gate polysilicon formed over a gate dielectric layer. ~~The gate electrode stack is formed on the surface of the silicon layer.~~ A cap layer in the top gate electrode surface is implanted with silicon or germanium. A plug of dielectric material, which may comprise a sidewall spacer material, fills a notch on the edges of the cap layer above the gate polysilicon and beneath a hard mask layer ~~that overlies~~ overlying the cap layer. The sidewall spacers cover ~~the sidewalls of the~~ gate electrode sidewalls and a portion of the plug to eliminate exposure of the gate polysilicon to avoid formation of spurious epitaxial growth of silicon nodules at the top corners of the gate electrode during the formation of raised source/drain regions. - -